REMARKS

Claims 1 to 14 are currently pending in the present application.

It is respectfully submitted that all of the presently pending claims are allowable, and reconsideration of the present application is respectfully requested.

With respect to paragraph six (6) of the Office Action, Applicants thank the Examiner for acknowledging the claim for foreign priority and for indicating that all certified copies of the priority documents have been received.

With respect to paragraph two (2) of the Office Action, the specification was objected to for not providing proper antecedent basis for the claimed subject matter. Specifically, the Office Action states that "[t]he specification fails to provide antecedent basis for the claim terminology 'computer readable medium' introduced in the April 14, 2005 amendment." (Office Action, pp. 2 to 3). While the objection may not be agreed with since the application discloses a computer readable medium, to facilitate matters, the paragraph beginning at page 8, line 19 (and ending at page 9, line 2) of the specification has been rewritten to substitute the phrase "A computer readable medium" for "An electrical storage medium." No new matter has been added. Approval and entry are respectfully requested, as is withdrawal of the objection.

With respect to paragraph four (4) of the Office Action, claims 10 to 12 were rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter. The Office Action states that "[t]he specification does not provide any definition for arrangement that would include a hardware element." (Office Action, p. 3). On the contrary, it is respectfully submitted that the specification does provide hardware elements corresponding to the control element for a micro controller, as provided for in the context of claims 10 to 12. Specifically, the control element is disclosed as a read-only memory or a flash memory (Specification, p. 1, lines 8 to 9), and is described as "implemented as a flash memory." (Specification, p. 9, lines 26 to 27; and p. 11, lines 22 to 23). Accordingly, it is respectfully submitted that claims 10 to 12 are directed to statutory subject matter.

Withdrawal of the rejections to these claims is therefore respectfully requested.

With respect to paragraph seven (7) of the Office Action, claims 1 to 8, 10 to 11, and 13 to 14 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,680,620 ("Ross").

As regards the anticipation rejections of the claims, to reject a claim under 35 U.S.C. § 102, the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. (See *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991)). As explained herein, it is respectfully submitted that the prior Office Action does not meet this standard, for example, as to all of the features of the claims. Still further, not only must each of the claim features be identically described, an anticipatory reference must also enable a person having ordinary skill in the art to practice the claimed subject matter. (See *Akzo, N.V. v. U.S.I.T.C.*, 1 U.S.P.Q.2d 1241, 1245 (Fed. Cir. 1986)).

As further regards the anticipation rejections, to the extent that the Office Action may be relying on the inherency doctrine, it is respectfully submitted that to rely on inherency, the Office must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; and see *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Int'f. 1990)). Thus, the M.P.E.P. and the case law make clear that simply because a certain result or characteristic may occur in the prior art does not establish the inherency of that result or characteristic.

Claim 1 relates to a computer readable medium having a program, the program performing a method for monitoring an execution of another program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller, the method including *causing the debug logic to trigger an exception* upon access to a specific address range during a program execution time, and *causing the debug logic to execute an exception routine* after the exception is triggered during the program execution time, in which *the access to the specific address range includes access to an illegal storage area*, and in which *the debug logic and its registers are operated in parallel to the program execution time* to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, *so as to provide a secure stack check without using the program execution time of the microprocessor.*

Ross does not identically disclose (or even suggest) all of the claimed features of claim 1. Ross merely refers to a processor with a debug register to notify one program of another program's access to a shared resource. (Ross, col. 2, lines 3 to 6). Specifically, the debug register of Ross is indicated as an integral component of the processor. (Ross, col. 2, line 67, to col. 3, line 2; and col. 4, lines 3 to 36). As a result, it is the processor of Ross that

monitors the breakpoint register, generates a device access interrupt, and executes a debug interrupt service routine. (Ross, col. 4, line 57, to col. 5, line 6). Thus, it is the processor of Ross, and not the debug register, which triggers the exception and executes an exception routine.

In direct contrast, claim 1 of the present application provides that the debug logic, and not the microprocessor, triggers an exception and executes an exception routine. Claim 1 further provides that the debug logic and its registers are operated in parallel to the program execution time, so as to provide a secure stack check without using the program execution time of the microprocessor. Since the processor of Ross must perform all of the monitoring, triggering, and executing functions, Ross does not disclose the feature of parallel operation of the debug register and the processor, such that the debug register functions without affecting the computing performance of the processor, as provided for in the context of the claimed subject matter. (See Specification, p. 5, lines 21 to 28).

In addition, Ross merely refers to monitoring access to a shared resource, in particular a peripheral device connected to the processor. (Ross, col. 2, lines 14 to 24). In this regard, Ross states that "[t]he address which is set as a breakpoint corresponds to the address which is called when access to the device is desired." (Ross, col. 4, lines 42 to 44). However, Ross does not disclose that the access to the specific address range includes access to an illegal storage area, as provided for in the context of claim 1.

Therefore, Ross does not identically disclose (or even suggest) all of the claimed features of claim 1, including the feature of *causing the debug logic to trigger an exception* upon access to a specific address range during a program execution time, and *causing the debug logic to execute an exception routine* after the exception is triggered during the program execution time, in which *the access to the specific address range includes access to an illegal storage area*, and in which *the debug logic and its registers are operated in parallel to the program execution time* to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, *so as to provide a secure stack check without using the program execution time of the microprocessor.*

Accordingly, it is respectfully submitted that claim 1 is allowable for at least these reasons. Claims 2 to 8 depend from and claim 1, and are therefore allowable for at least the same reasons as claim 1.

Claim 10 relates to a control element for a micro controller, and includes features analogous to those of claim 1. Accordingly, it is respectfully submitted that claim 10 is allowable for essentially the same reasons as claim 1, as is its dependent claim 11.

Claim 13 relates to a micro controller, including at least one microprocessor and a debug logic, and includes features analogous to those of claim 1. Accordingly, it is respectfully submitted that claim 13 is allowable for essentially the same reasons as claim 1, as is its dependent claim 14.

Withdrawal of these rejections is therefore respectfully requested.

With respect to paragraph eight (8) of the Office Action, claim 9 was rejected under 35 U.S.C. § 103(a) as unpatentable over Ross, in view of U.S. Patent No. 6,535,811 ("Rowland et al.").

In rejecting a claim under 35 U.S.C. § 103(a), the Office bears the initial burden of presenting a *prima facie* case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim features. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

As essentially explained above, Ross does not disclose or even suggest all of the features of claim 1. Further, it is respectfully submitted that even if it were proper to combine Ross and Rowland, as suggested by the Office Action (which is not conceded), Rowland does not cure -- and is not asserted to cure -- the critical deficiencies of the Ross reference.

Accordingly, dependent claim 9 is allowable for essentially the same reasons as its base claim, since the Rowland reference does not cure -- and is not asserted to cure -- the critical deficiencies of the primary Ross reference.

Withdrawal of this obviousness rejection is therefore respectfully requested.

With respect to paragraph nine (9) of the Office Action, claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over Ross, in view of what the Office Action characterizes as Admitted Prior Art ("APA").

Applicants first note that the Office Action again relies on the BACKGROUND INFORMATION Section of the present application. In this regard, it is noted that while certain published information may represent prior art (namely, any cited patents that are prior art), the information concerning the "debug logic triggering" may represent internal Bosch information.

Regardless of the Office Action's characterization of the "Background Information", it is respectfully submitted that the asserted combination does not render unpatentable claim 12 for at least the following reasons. As explained above, Ross does not disclose or even suggest all of the features of claim 10. Further, the "Background Information" does not cure -- and is not asserted to cure -- the critical deficiencies of the Ross reference.

Accordingly, it is respectfully submitted that claim 12 is allowable for the same reasons as claim 10, since the "Background Information" does not cure -- and is not asserted to cure -- the critical deficiencies of the Ross reference.

Withdrawal of this obviousness rejection is therefore respectfully requested.

It is therefore respectfully submitted that claims 1 to 14 are allowable.

Conclusion

It is therefore respectfully submitted that all of the presently pending claims are allowable. It is therefore respectfully requested that the objections and rejections be withdrawn, since all issues raised have been addressed and obviated. An early and favorable action on the merits is respectfully requested.

Respectfully submitted,

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